CLAIMS:

1. A data handling device, the device comprising:

- a data memory (10) with an address input and a data output, for outputting multi-bit words addressed by addresses from the address input, the data memory (10) having a structure that gives rise to potential errors at correlated positions in words from a group of words with addresses within a group of addresses;

- an erasure memory unit (16) coupled to the address input and arranged to store bit position information associated with the group of the words, and to output the bit position information when a word from the group for which bit position information is stored is addressed in the data memory (10);

- an error correction and detection unit (12) coupled to the data output of the data memory (10) and to the erasure memory unit (16), and arranged to correct words from the data memory (10), using error erasure for bits at bit positions selected by the bit position information from the erasure memory unit (16), for the groups to which the words belong.

2. A data handling device according to Claim 1, wherein the erasure memory unit (16) comprises an associative memory (30, 32, 34), comprising one or more storage locations for storing bit information for no more than a subset of all groups of words in the data memory (10), the one or more storage locations being associatively addressable with the address from the address input of the data memory (10).

3. A data handling device according to Claim 2, comprising a cache management unit(18) arranged to select a storage location from the associative memory (30, 32, 34) for reuse for bit position information for a particular group, on detecting an address of a word from that particular group on the address input when no storage location is in use for that particular group.

4. A data handling device according to Claim 2, wherein erasure memory unit (16) is arranged to replace bit position information in one of storage locations by bit information for a particular group on detecting an address of a word from that particular

group on the address input conditionally if an error is detected in the word form the particular group that is read from the data memory, when no storage location is in use for that particular group.

5. A data handling device according to Claim 2, wherein the associative memory comprises a storage element (32) for bit information for a single group only.

6. A data handling device according to Claim 1, wherein the erasure memory unit (16) is arranged to store validation information associated to the group of the words and to enable use of the bit position information by the error correction and detection circuit only if validated by the validation information, the erasure memory unit (16) being arranged to set the validation information for a particular group to an enabling value only if errors have been detected during at least a plurality of read operations of a word or words from the particular group.

7. A data handling device according to Claim 1, comprising a retry circuit coupled to the error correction and detection circuit (12) and the address input of the data memory (10) and arranged to respond to detection of an uncorrectable error for a word from a particular group, by applying the address of at least one other word from the particular group to the data memory, the erasure memory unit (16) being arranged to store bit information for the particular group that is derived from at least one other word.

8. A data handling device according to Claim 1, wherein the erasure memory unit (16) is arranged to retrieve the bit information using only a part from an address that is applied to the data input of the data memory, wherein said part identifies the group to which the word belongs, the erasure memory unit being reconfigurable to adapt said part to a type of data memory used.

9. A data handling device according to Claim 1, wherein the data memory (10) is a NAND flash memory, the groups containing to words that have bit positions for which data is stored in transistors whose main current channels are connected in series.

10. A method of reading multi-bit data words from a data memory (10), the method comprising:

- keeping bit position information associated with at least one group of the words in storage (16), in association with an identification of the group;
- outputting the bit position information when a word from the group for which bit position information is stored is addressed in the data memory (10);
- correcting words from the data memory under erasure of bits at bit positions selected by the bit position information from the erasure memory unit (16).